LESS: LOOP NEST EXECUTION STRATEGY FOR SPATIAL ARCHITECTURES

Amalee Wilson - University of Alabama Birmingham
Swapna Raj, Kermin Fleming - Intel
MOTIVATION

- Conventional architectures challenged to reach exascale
- Reconfigurable spatial architectures, e.g. FPGAs, can help

Perfect World

High level code user is familiar with \[\rightarrow\text{\textit{sorcery}}\] Optimized executable for target architecture
OVERALL STRATEGY

Simple Example Program:
- OuterLoop1
- InnerLoop1
- InnerLoop2
- OuterLoop2
- InnerLoop3

Best solution
- OuterLoop1
  nest

Best solution
- OuterLoop2
  nest

Best solution for full program
OFFLOADING CHILD LOOPS

- Find best whole loop implementation, e.g. figure 1
- Find best child loop implementations, e.g. figure 2
- Which gives better performance?

Example loop:
LoopA
  LoopB
  LoopC

Figure 1
1 x A
4 x B
6 x C

Figure 2
A on host
8 x B
12 x C
OFFLOADING STRATEGY

- Unroll to exhaust fabric per loop
- Remove copies based on marginal value

**Example loop:**

- LoopA
  - LoopB
  - LoopC

Reduce total area by removing least valuable loop
PRELIMINARY RESULTS

Configuration Time:

- $n \times 10^1$
- $n \times 10^2$
- $n \times 10^4$
- $n \times 10^6$
- $n \times 10^7$
- host

Speedup vs. Area
THANK YOU!