Call for Papers

Fifth International Workshop on Heterogeneous High-performance Reconfigurable Computing (H^2RC)

November 17, 2019
(All Day Sunday)

Held in conjunction with SC19: The International Conference for High Performance Computing, Networking, Storage and Analysis

In cooperation with

http://h2rc.cse.sc.edu

New for 2019: Accepted Papers will be indexed and published in the IEEE Digital Library though TCHPC

Submission Deadline
~~August 15, 2019~~ **~~August 23, 2019 (extended)~~ August 26, 2019 (extended)**
(8-page full papers or 4-page extended abstract, see below)

As conventional von-Neumann architectures are suffering from rising power densities, we are facing an era with **power**, **energy efficiency**, and **cooling** as first-class constraints for scalable HPC. FPGAs can tailor the hardware to the application, avoiding overheads and achieving higher hardware efficiency than general-purpose architectures. Leading FPGA manufacturers have recently made a concerted effort to provide a range of higher-level, easier-to-use high-level programming models for FPGAs, and much of the work in FPGA-based deep learning is built on these frameworks.

Such initiatives are already stimulating new interest within the HPC community around the potential advantages of FPGAs over other architectures. With this in mind, this workshop, now in its fifth year, brings together HPC and heterogeneous-computing researchers to demonstrate and share experiences on how newly-available high-level programming models, including OpenCL, are already empowering HPC software developers to directly leverage FPGAs, and to identify future opportunities and needs for research in this area.

Submission Tracks and Contribution Selection

Submissions are solicited for two tracks:

- **Track 1:** Full-length papers (8 pages) for 25-minute oral presentation and publication in proceedings archived by IEEE.
- **Track 2:** Extended abstracts (4 pages) for 15-minute oral presentation without publication.

Track 1 is targeted for technical papers containing a high level of implementation detail and analysis discussion of experimental results. Track 1 is suited for members of the academic and national lab community who prefer to have their work peer-reviewed, indexed and archived by IEEE.

Track 2 is targeted for industrial contributions that describe new capabilities and opportunities offered by emerging technologies and products or work in progress presentations by the academic and national lab community. The emphasis of this track is to initiate a discussion with the audience.

All submissions are reviewed and evaluated by at least three members of our technical program committee. From the TPC evaluation of each submission, the organizing committee will select papers for presentation based on a criteria that is **equally weighted** between scientific merit and level of interest and relevance to the HPC community.

Submission Topics

Submissions are solicited that explore the state of the art in the use of FPGAs in heterogeneous high-performance compute architectures and, at a system level, in data centers and supercomputers. FPGAs may be considered from either or both the distributed, parallel and composable fabric of compute elements or from their dynamic reconfigurability. We particularly encourage submissions which focus on the mapping of algorithms and applications to heterogeneous FPGA-based systems as well as the overall impact of such architectures on the compute capacity, cost, power efficiency, and overall computational capabilities of data centers and supercomputers. Submissions may report on theoretical or applied research, implementation case studies, benchmarks, standards, or any other area that promises to make a significant contribution to our understanding of heterogeneous high-performance reconfigurable computing and will help to shape future research and implementations in this domain. A non-comprehensive list of potential topics of interest is given below:

1. Improvement of performance or efficiency of HPC or data center applications with FPGAs
2. System integration of FPGAs in clouds and HPC systems
3. Leveraging reconfigurability
4. Benchmarks
6. Programming languages, tools, and frameworks
7. Future-gazing

Submission Guidelines

Full papers (Track 1)
Authors should submit original contributions of up to 8 pages in PDF format using the SC19 Linklings portal (https://bit.ly/2MugOkk), which is also linked from the H2RC website (https://h2rc.cse.sc.edu). Submissions must be formatted as single-spaced, double-column, A4 pages without page numbers following the IEEE Conference Proceedings format, including figures, tables, and references. H2RC uses a single blind review process. We support the SC reproducibility initiative and highly encourage authors to add an artifact description/artifact evaluation appendix of up to 2 additional pages to their paper. All accepted papers will be published in the IEEE TCHPC Proceedings and will be available free of charge and indexed by the IEEE Xplore digital library.

Talk proposals (Track 2)
To apply for a talk authors should submit a 4-page extended abstract. The extended abstract will peer-reviewed and used for deciding on the acceptance of a presentation assignment of a presentation slot, but will not be published in the proceedings. The papers shall follow the same formatting instructions as the full papers and have also to be submitted using the Linklings system.

Important dates:

Submission Deadline:	~~August 15, 2019~~ **August 23, 2019 (extended)**
Acceptance Notification:	September 15, 2019
Camera-ready Manuscripts Due:	October 11, 2019
Workshop Date:	November 17, 2019

Workshop Format
H^2RC is a full-day Sunday workshop. It will be comprised of:
- Keynote and invited talks
- Talks selected among paper submissions
- Panel discussion on research opportunities and needs

Workshop Organizers:

Jason D. Bakos, University of South Carolina
Michaela Blott, Xilinx
Franck Capello, Argonne National Lab
Torsten Hoefler, ETH Zurich
Christian Plessl, Paderborn University

Technical Program Committee:

David Andrews, University of Arkansas
Rizwan Ashraf, Oak Ridge National Laboratory
Paul Chow, University of Toronto
Hans Eberle, Nvidia

Ken Eguro, Microsoft Research
Xin Fang, Northeastern University
Alan George, University of Pittsburgh
Christoph Hagleitner, IBM
Martin Herbordt, Boston University
Zheming Jin, Argonne National Laboratory
Andreas Koch, TU Darmstadt
Miriam Leeser, Northeastern University
Tiffany Mintz, Oak Ridge National Laboratory
Viktor Prasanna, University of Southern California
Yaman Umuroglu, Xilinx Research