

CFD Acceleration with FPGA



Launching byteLAKE's CFD Suite

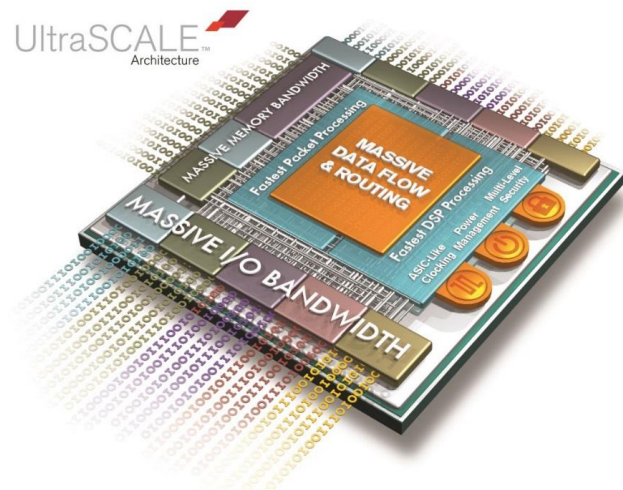


Krzysztof Rojek, CTO at byteLAKE, PhD, DSc at Czestochowa University of Technology

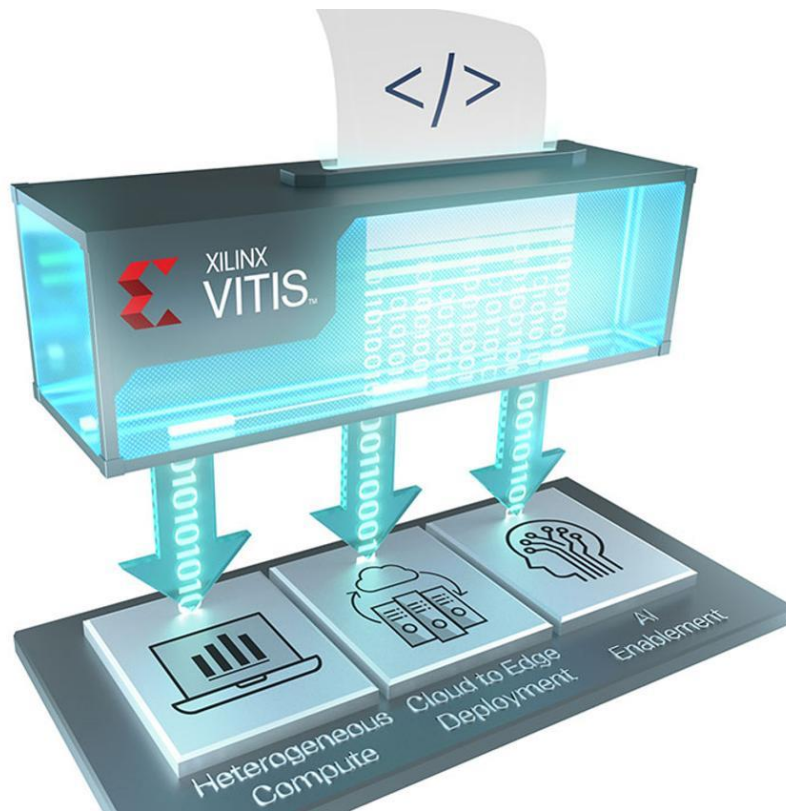
Jamon Bowen, Director, Segment Marketing and Planning at Xilinx

FPGAs – The Ultimate Parallel Processing Device

- › No predefined instruction set or underlying architecture
- › Developer customizes the architecture to his needs
 - » Custom datapaths
 - » Custom bit-width
 - » Custom memory hierarchies
- › Excels at all types of parallelism
 - » Deeply pipelined (e.g. Video codecs)
 - » Bit manipulations (e.g. AES, SHA)
 - » Wide datapath (e.g. DNN)
 - » Custom memory hierarchy (e.g. Data analytics)
- › Adapts to evolving algorithms and workload needs



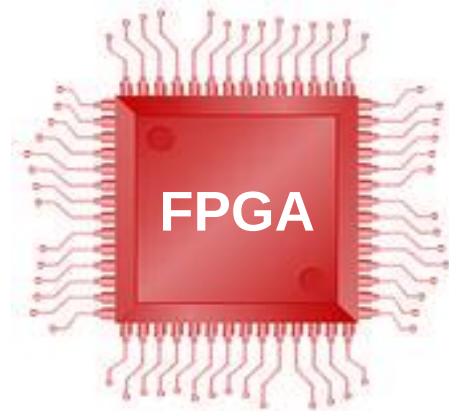
VITIS – Heterogeneous compute development environment



Using C, C++ or OpenCL to Program FPGAs

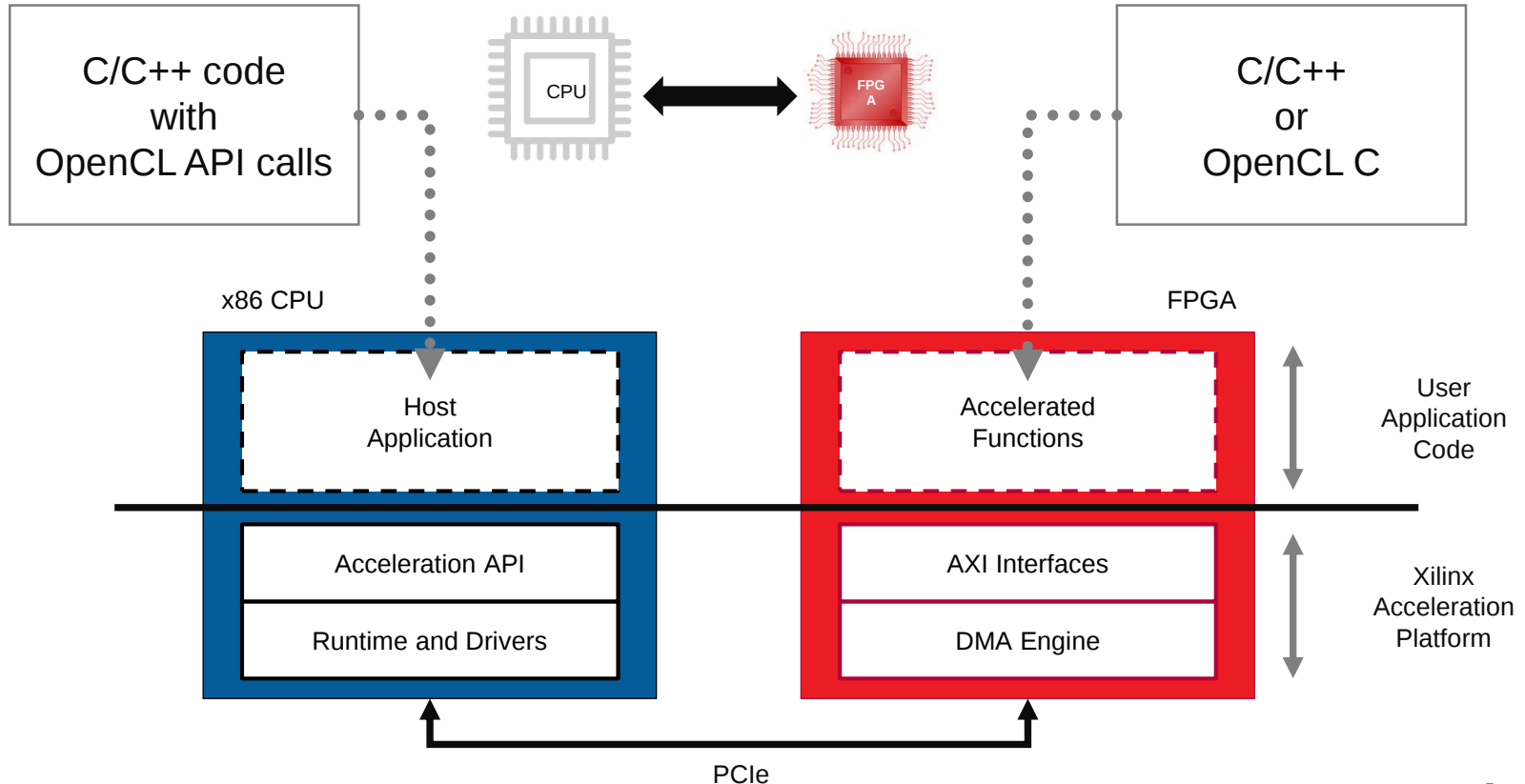
```
loop_main:for(int j=0;j<NUM_SIMGROUPS;j+=2) {  
  loop_share:for(uint k=0;k<NUM_SIMS;k++) {  
    loop_parallel:for(int i=0;i<NUM_RNGS;i++) {  
      mt_rng[i].BOX_MULLER(&num1[i][k],&num2[i][k],ratio4,ratio3);  
      float payoff1 = expf(num1[i][k])-1.0f;  
      float payoff2 = expf(num2[i][k])-1.0f;  
      if(num1[i][k]>0.0f)  
        pCall1[i][k]+= payoff1;  
      else  
        pPut1[i][k]-=payoff1;  
      if(num2[i][k]>0.0f)  
        pCall2[i][k]+=payoff2;  
      else  
        pPut2[i][k]-=payoff2;  
    }  
  }  
}
```

Compile

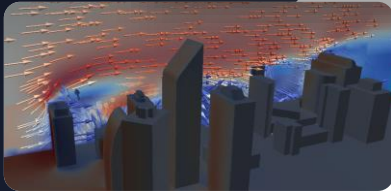
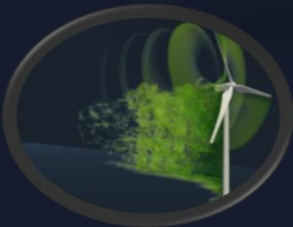
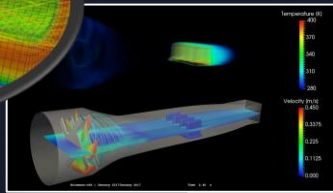
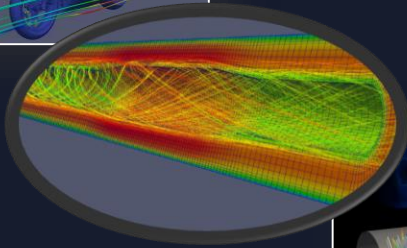
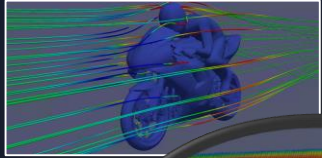


- › Xilinx pioneered C to FPGA compilation technology (aka “HLS”) in 2011
- › Enables “Software Programmability” of FPGAs
- › Includes open source collection of optimized HLS libraries

Software Programmability: FPGA Development in C/C++



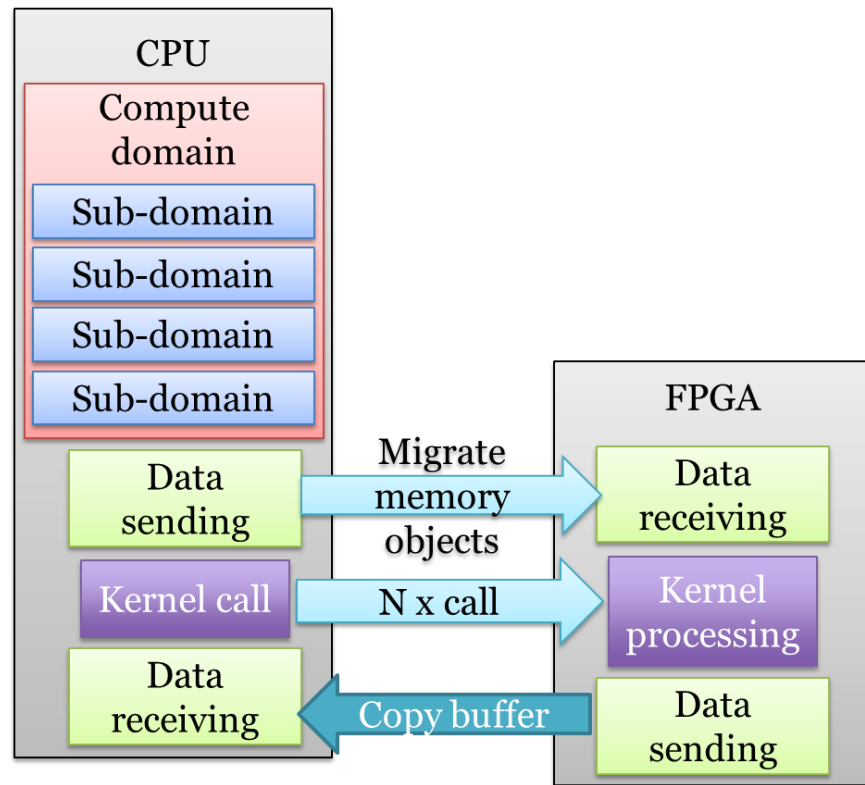
CFD, Computational Fluid Dynamics



- › Numerical analysis and algorithms to solve fluid flows problems.
- › Model fluids density, velocity, pressure, temperature, and chemical concentrations in relation to time and space.
- › Typical applications: weather simulations, aerodynamic characteristics modelling and optimization, flow around buildings simulations etc.

Architecture

- › The compute domain is divided into 4 sub-domains
- › Host sends data to the FPGA global memory
- › Host calls kernel to execute it on FPGA (kernel is called many times)
- › Each kernel call represents a single time step
- › FPGA sends the output array back to host

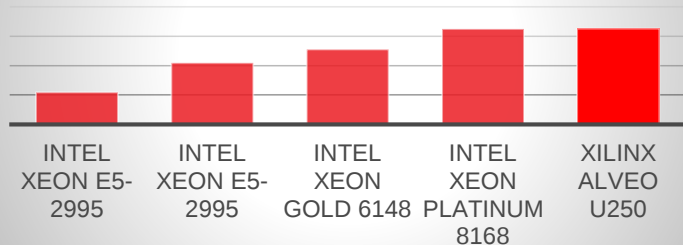


Alveo Optimizations

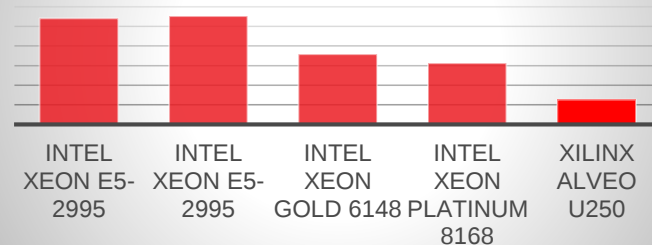


Conclusions

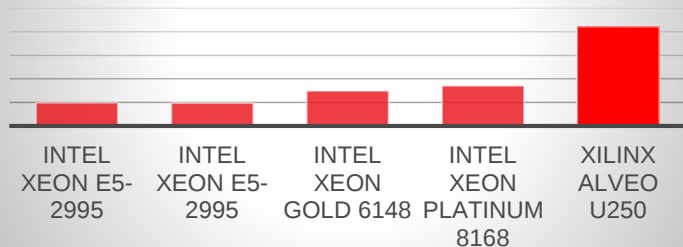
Performance (the higher the better)



Energy (the lower the better)



Performance/W (the higher the better)



- Up to 4x more performance
- Up to 80% lower energy consumption
- Up to 6x more performance/Watt

Launching byteLAKE's CFD Suite (BCS)

› Highlights

- › Collection of Alveo Optimized CFD Workloads
- › Acceleration = Faster Results
- › Green Computing = Improved Efficiency
- › Microservices = Quick Start
- › Excellent TCO = Cost Saving
- › AI Driven Approach



First Microservices Launching Today

- › Advection
- › Thomas Algorithm (linear algebra module)
- › Low barrier entry
 - » Scalable on demand
 - » As a Service / Cloud
 - » On-premise



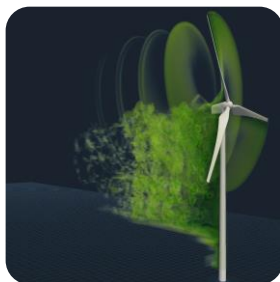
Way Forward

byteLAKE's
CFD Suite
(GCS)

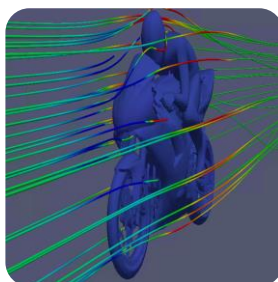


More Microservices (roadmap)

Green Energy



Automotive



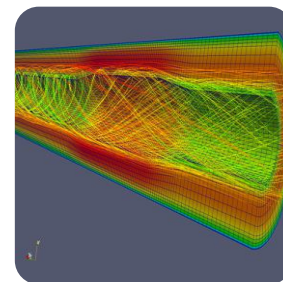
Construction



Chemistry



Oil & Gas



Use Case
Specific

Highly Optimized

AI Driven

byteLAKE at SC19

HPC and AI Convergence

- CFD Acceleration with FPGA (workshop)
- byteLAKE's CFD Suite (Alveo optimized, demo)
- Leveraging AI for Reforestation Efforts and AI Training Acceleration (demo)

Booth:

H2RC, 607



Lenovo



Denver, CO, Colorado Convention Center, Nov 17-21

[byteLAKE.com](https://byteLAKE.com/en/SC19)
[/en/SC19](https://byteLAKE.com/en/SC19)



Thank You

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