Microdisk Cavity FDTD Simulation on FPGA using OpenCL

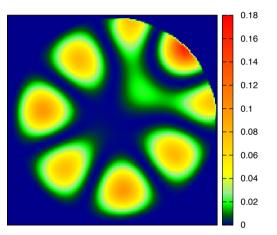
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- Microdisk cavity in perfect metallic environment
 - Well studied nanophotonic device
 - Point-like time-dependent source (optical dipole)
 - Known analytic solution (whispering gallery modes)

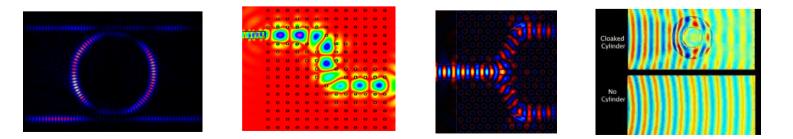




experimental setup: microdisk cavity

result: energy density

• Simulations can help to investigate other nanophotonic setups



Computational Nanophotonics

- Physics: Maxwell's partial differential equations
 - Electric field E
 - Magnetic field H
 - Material constants (electric permittivity ε, magnetic permeability μ)

$$\frac{\partial H}{\partial t} = -\frac{1}{\mu} \nabla \times E - \frac{1}{\mu} (M_{source} + \sigma^* H)$$
$$\frac{\partial E}{\partial t} = \frac{1}{\epsilon} \nabla \times H - \frac{1}{\epsilon} (J_{source} + \sigma E)$$

- Simulation: FDTD stencils
 - Stencil for dielectric material in 2D

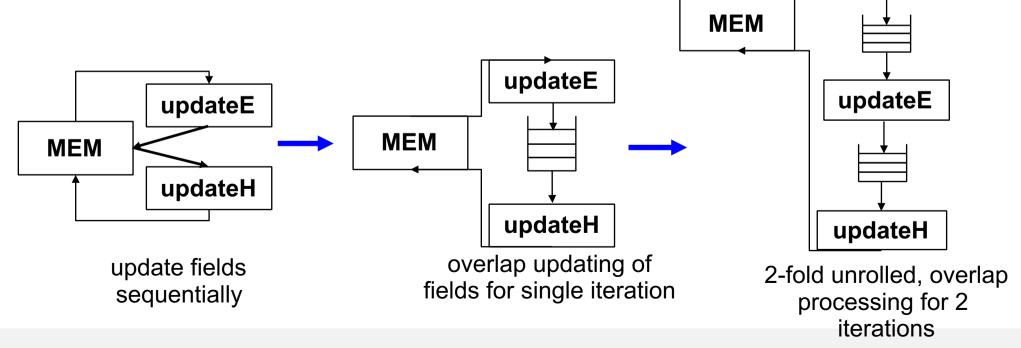
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updateE(*ex, *ey, *hz) {
    ex[x,y] = ca * ex[x,y] + cb * (hz[x,y] - hz[x,y-1]);
    ey[x,y] = ca * ey[x,y] + cb * (hz[x-1,y] - hz[x,y]);
}
updateH(*ex, *ey, *hz) {
    hz[x,y] = da * hz[x,y] + db * (ex[x,y+1] - ex[x,y] + ey[x,y] - ey[x+1,y]);
}
```

FPGA Pipeline for FDTD

updateE

updateH

- Inside time step
 - Regular + parallel update operations
 - Can form customized loop pipeline on FPGA
 - Locality + predictable memory access
 - Can prefetch and stream data
- E and H are must be updated alternately (leap-frog)
 - Reusing local results is key to performance
 - Unrolling several time steps increases computational intensity



OpenCL for FPGAs

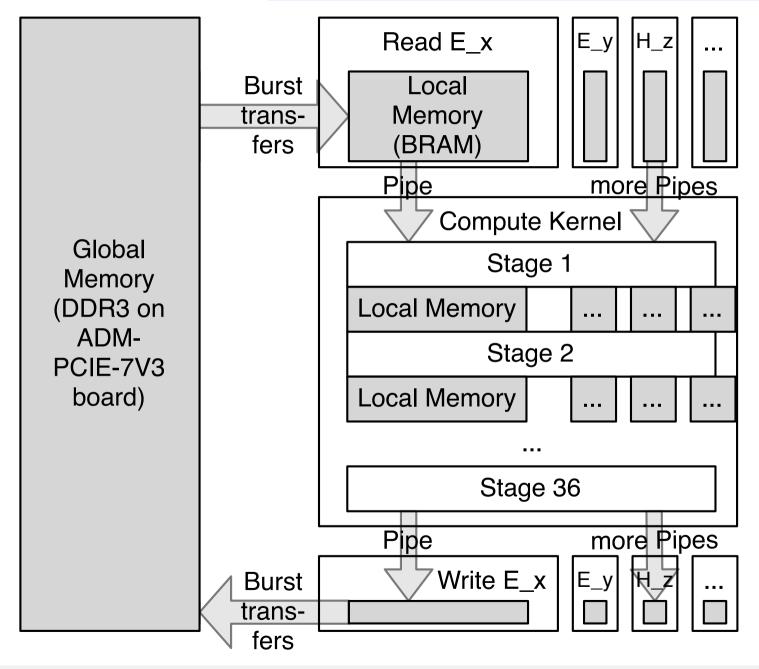
- OpenCL
 - Covers parallelism and awareness of memory locations
 - Base of familiar developers (mostly GPU)
 - Suitable to generate competitive FDTD design on FPGA?
- OpenCL-based SDAccel tool flow
 - OpenCL source-to-source transformation
 - Vivado HLS step
 - Vivado synthesis place + route
 - SDAccel Version 2016.1
- Target system
 - ADM-PCIE-7V3 board with Xilinx Virtex-7 XC7VX690T + 2x 8GB DDR3 memory

Design Steps

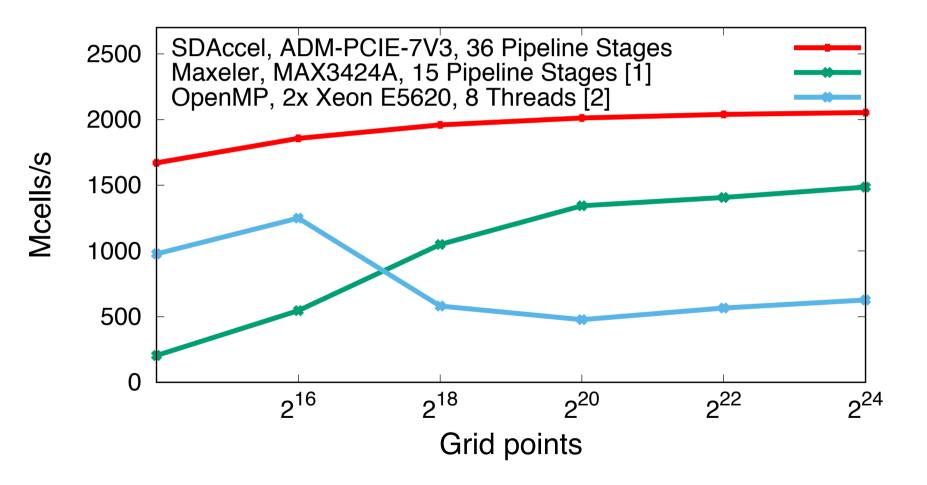
- 1. Wrap main loop into OpenCL kernel
 - First FPGA design up and running after few hours
 - ~1000x slower than CPU
- 2. Generate FPGA pipeline for E and H updates
 - Burst transfers to local memory
 - Compute from local memory
 - Pipeline main loop with low initiation interval
- 3. On the way...
 - Separate compute + transfer kernels, coupled through pipes
 - Code transformations in compute kernel
- 4. Unroll as many time steps as resources permit
 - Allow data reuse
 - Instantiate many individual buffers



OpenCL-based FPGA Design



- 36 pipeline stages, initiation interval 2
- 140MHz (down from original target 200MHz)



- Resulting design with OpenCL is very competitive
- Code is adapted to FPGA target and current tool capabilities
 - Much lenghty boilerplate may go away with maturing tools and better understanding of them
 - Performance portability not explored (currently design with singe work-item)

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Thank you!

