P4-to-FPGA: High Performance Reconfigurable Networking

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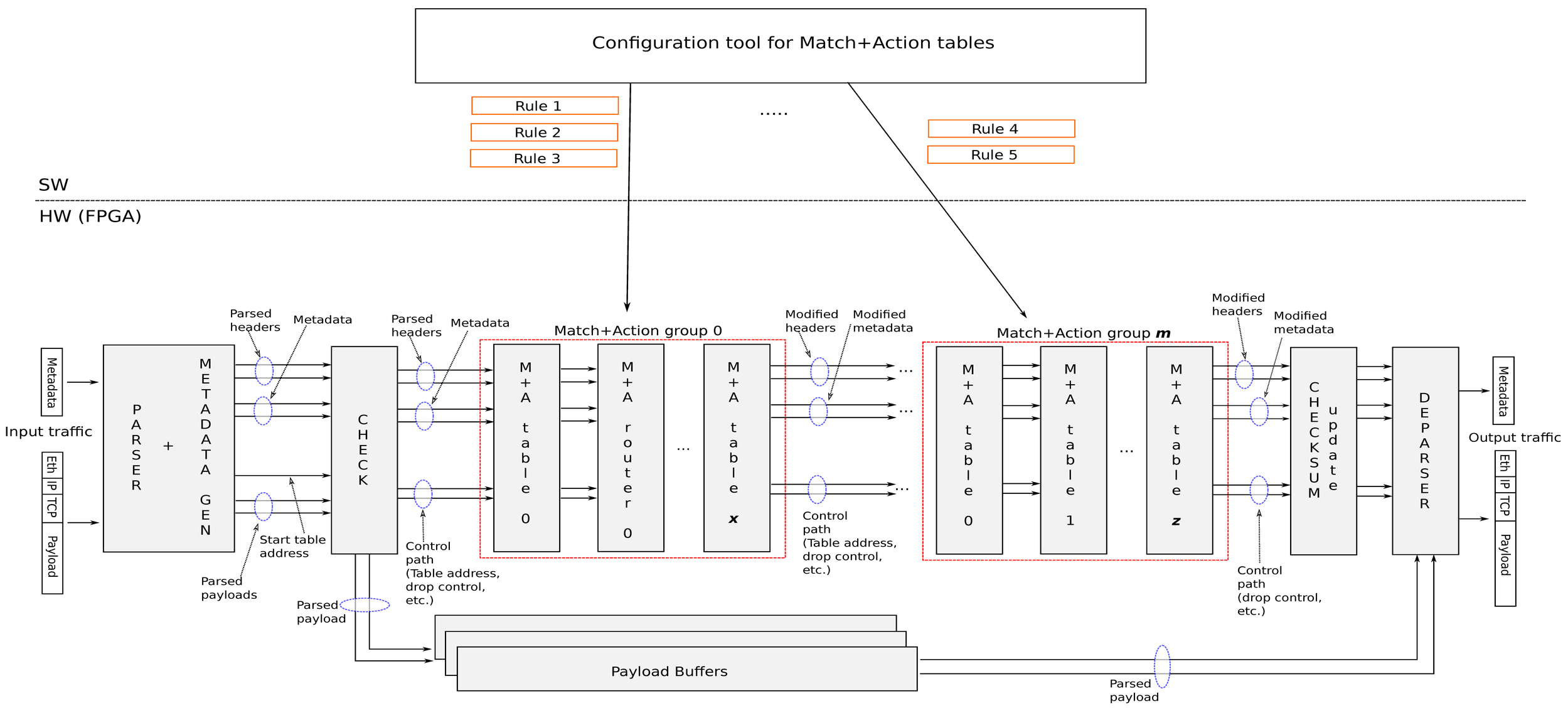
- Direct generation of network device from P4 language
- Generated VHDL modules are capable to process 100 Gbps
- Three modules:
  - Parser - transforms network packet to the set of protocols headers
  - Deparser - transforms the set of protocols headers to network packet
  - Match+Action pipeline - implements the required desicion-making functionality

Structure of Generated Pipeline



Experiments

- Three use cases were tested on Virtex 7 FPGA:
  - IPv4 Filter - filtering based on IPv4 address
  - IPv4+IPv6 Filter - extends the previous with IPv6 protocol
  - Full Filter - extends the previous with the ability to tag the traffic (MPLS/VLAN)