

Motivation

The PyDAC runtime for a FPGA-based heterogeneous architecture demonstrated that algorithms using the Divideand-Conquer design pattern can balance multiple ---sometimes conflicting --- system goals.



Key Question:

Can the same success be extended to another class of applications that use, for example, the Wavefront design pattern?

To test this, we left the hardware unchanged and investigated four well-known wavefront algorithms: LU decomposition, QR decomposition, Cholesky decomposition and matrixmatrix multiplication.

Success is defined as:

- A simple application/runtime interface
- Efficient use of the memory subsystem

(The hardware does not change so power and resilience are not impacted by these tests.)



- Match and Post method for memory access
- Object store and no linear array of memory

Currently implemented in software but part of heterogeneous hardware

The Waverun Programming Model for FPGA-Based Heterogeneous Architectures Abhi D.R. and Ron Sass

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Examples



Runtime

- Provides simple user interface Schedule and Gather methods to schedule the task and gather the result
- One program for different types of cores
- Manages memory keys

Programmer responsibility:

- Simple object-oriented interface to runtime
- Provide function based on the index
- Block of input data via Python method



Results

A simple application/runtime interface with two user methods is implemented

Cholesky Decomposition Amat=np.random.randint(num,size=(row,column)) myapp=dpbtrf(Amat, block) myapp.schedule(row/block) myapp.gather('Result') **Matrix Multiplication** Amat=np.random.randint(num,size=(row,column)) Bmat=np.random.randint(num,size=(row,column)) myapp=dgemm((Amat,Bmat),block) myapp.schedule(row/block) myapp.gather('Result') User application using the runtime interface

Cholesky, LU, QR, and Matrix multiplication algorithms were implemented using "wavefront" design pattern

Cholesky, LU, and QR works well with point-point computation

But proves inefficient with blocking



Results of matrix multiplication with blocking

Hardware memory subsystem is tested for transaction bandwidth of range 20k-40k. The runtime efficiently uses the system by generating keys of similar range.

Background

Pydac previously implemented: Divide and conquer Proven to be efficient for certain algorithms

B. Huang, R. Sass, N. Debardeleben and S. Blanchard, "Harnessing Unreliable Cores in Heterogeneous Architecture The PyDac Programming Model and Runtime," 2014 44th Annual IEEE/IFIP International Conference on Dependable Systems and Networks, Atlanta, GA, 2014, pp. 744-749.

Design Patterns Intel TBB (Parallel patterns)

- Divide and Conquer
- Wavefront
- Agglomeration
- Elementwise
- Reduction

Future Work

- Developing graph related algorithms for waverun
- Testing the runtime with the heterogeneous hardware