The Case for Custom Parallel Memories: an Application-Centric Analysis

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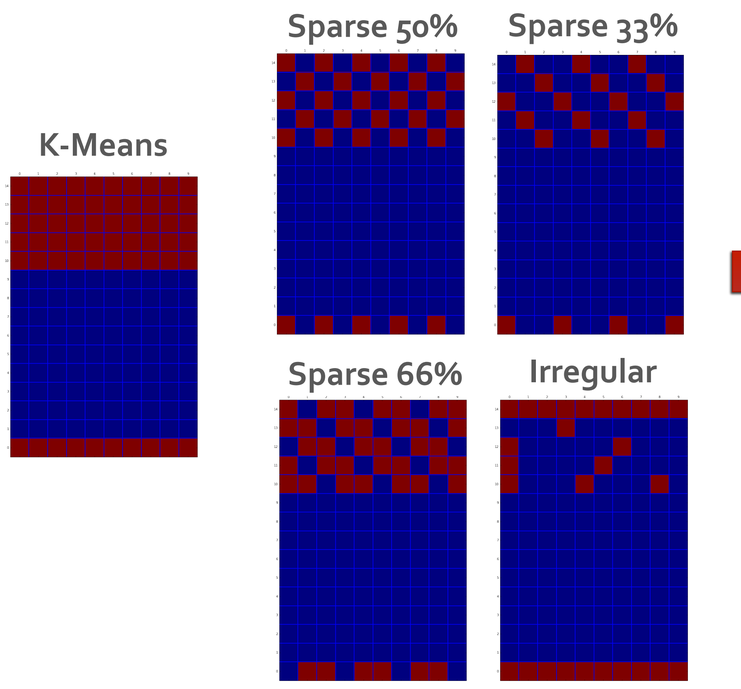
The main idea

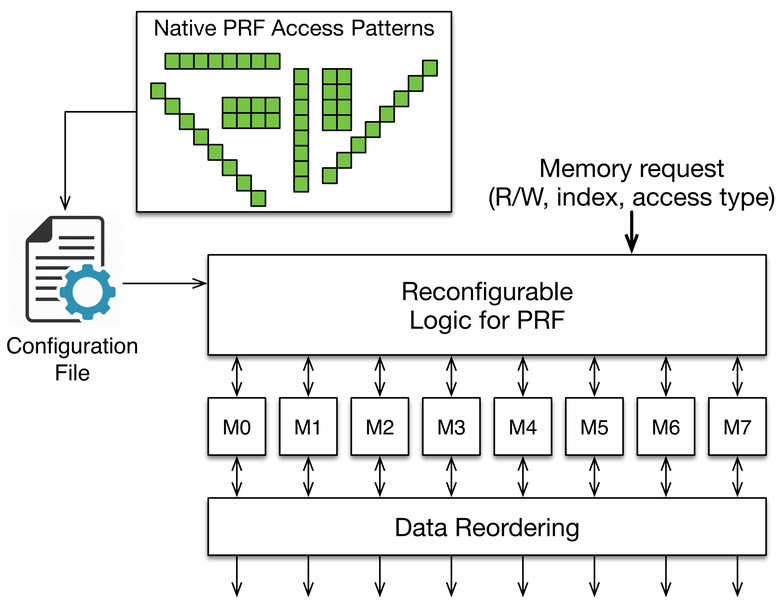
For many applications, the performance bottleneck is memory throughput. In this work, we propose to use FPGAs for building parallel custom memory systems to accelerate such applications.

Application Access Patterns



Parallel Reconfigurable Memory

We use the PRF [1] as a 2D reconfigurable scratchpad parallel memory.



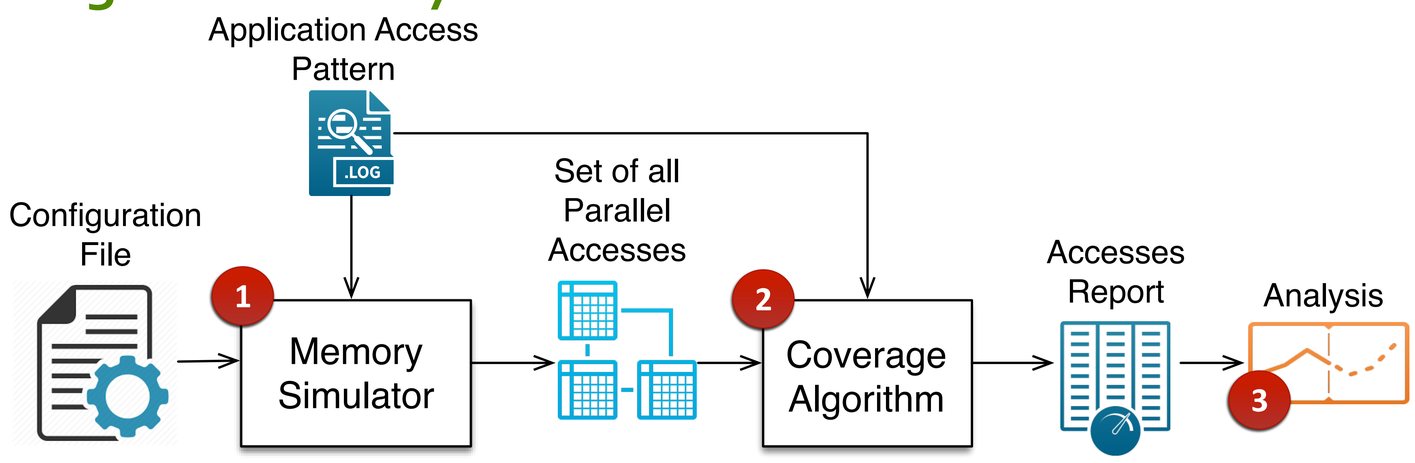
A configuration for the PRF specifies the number of memory used in parallel and (the subset of) the patterns to be supported.

Metrics

$$\text{Speedup} = \frac{\#\text{SequentialAccesses}}{\#\text{ParallelAccesses}}$$ Gain from using a parallel memory

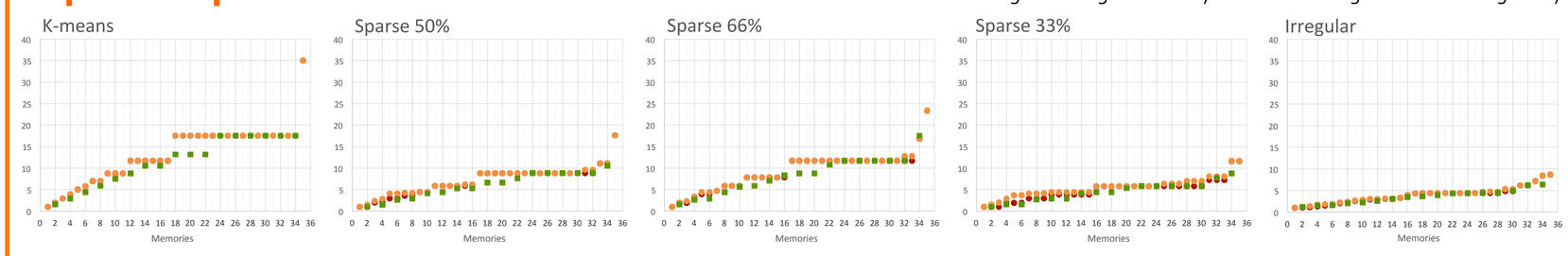
$$\text{Efficiency} = \frac{\text{ElementsReadByApplication}}{\text{ElementsReadByParallelMemory}}$$ Penalty from using a parallel memory

Configuration Analysis



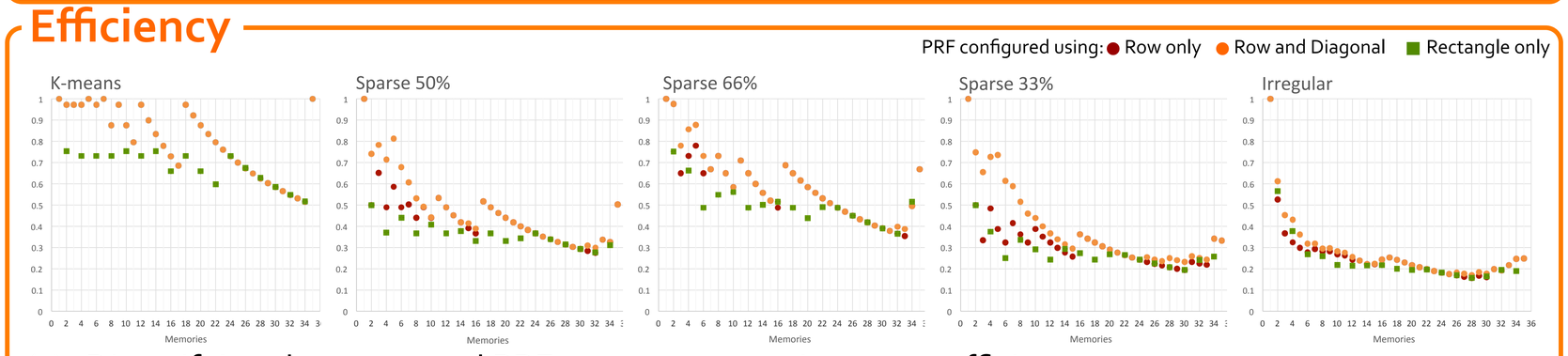
1. The memory simulator generates the possible parallel accesses. The number of elements accessible in each parallel access depends on the number of memories used in parallel.
2. The Coverage algorithm, which solves the minimum set cover using Integer Linear Programming (ILP), is used to find the minimum number of parallel accesses (as generated by the memory simulator) that cover the memory access pattern of the application.
3. The list of parallel accesses obtained by the ILP solver is used to compute **speedup** and **efficiency** of the analyzed configuration.

Speed-up



(1) Parallel memory systems provide speed-up in all cases.
(2) Combining multiple, different PRF access patterns is beneficial for speed-up.
(3) The "staircase" effect indicates that there are multiple configurations possible to achieve the same speed-up.

Efficiency



(1) Diversifying the supported PRF access patterns increases efficiency.
(2) The design of a parallel memory system should maximize efficiency to avoid useless memory ops; thus, for the same speed-up, the design with the highest efficiency should be selected.

Take Home Message

Using parallel memories is not trivial. Our approach offers an integrate semi-automatic approach to customize the memory system for your application, and evaluate its potential performance.

More info ?

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