

C-based Synthesis of Area-Efficient Accelerators for OpenMP Worksharing Loops

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```
#pragma omp parallel for shared(A,B,C) private(j,k) \  
    num_threads(4) schedule(static)  
for(i=0; i<N; i++){  
    for(j=0; j<N; j++){  
        for(k=0; k<N; k++)  
            C[i][j] = C[i][j] + A[i][k] * B[k][j];  
    }  
}
```

Motivation

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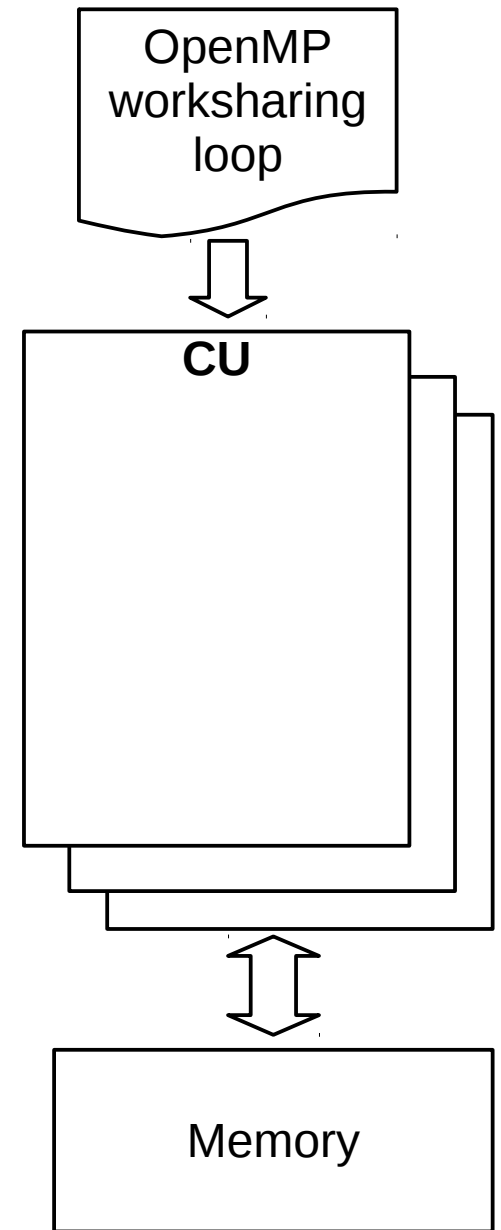
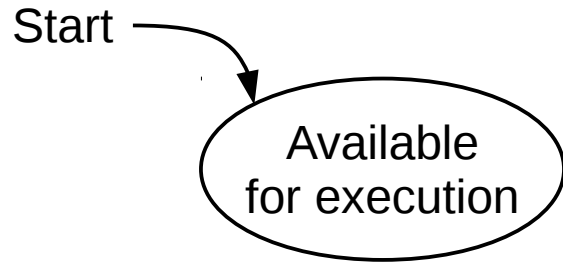
Exploitation of Thread-Level Parallelism (TLP) in High-Level Synthesis:

- HPC usage scenarios demand higher throughput
- FPGA sizes continue growing
 - Allows for duplicated datapaths
- Low utilization in HLS-generated compute units (CU) observed
 - Improve with dynamic thread interleaving

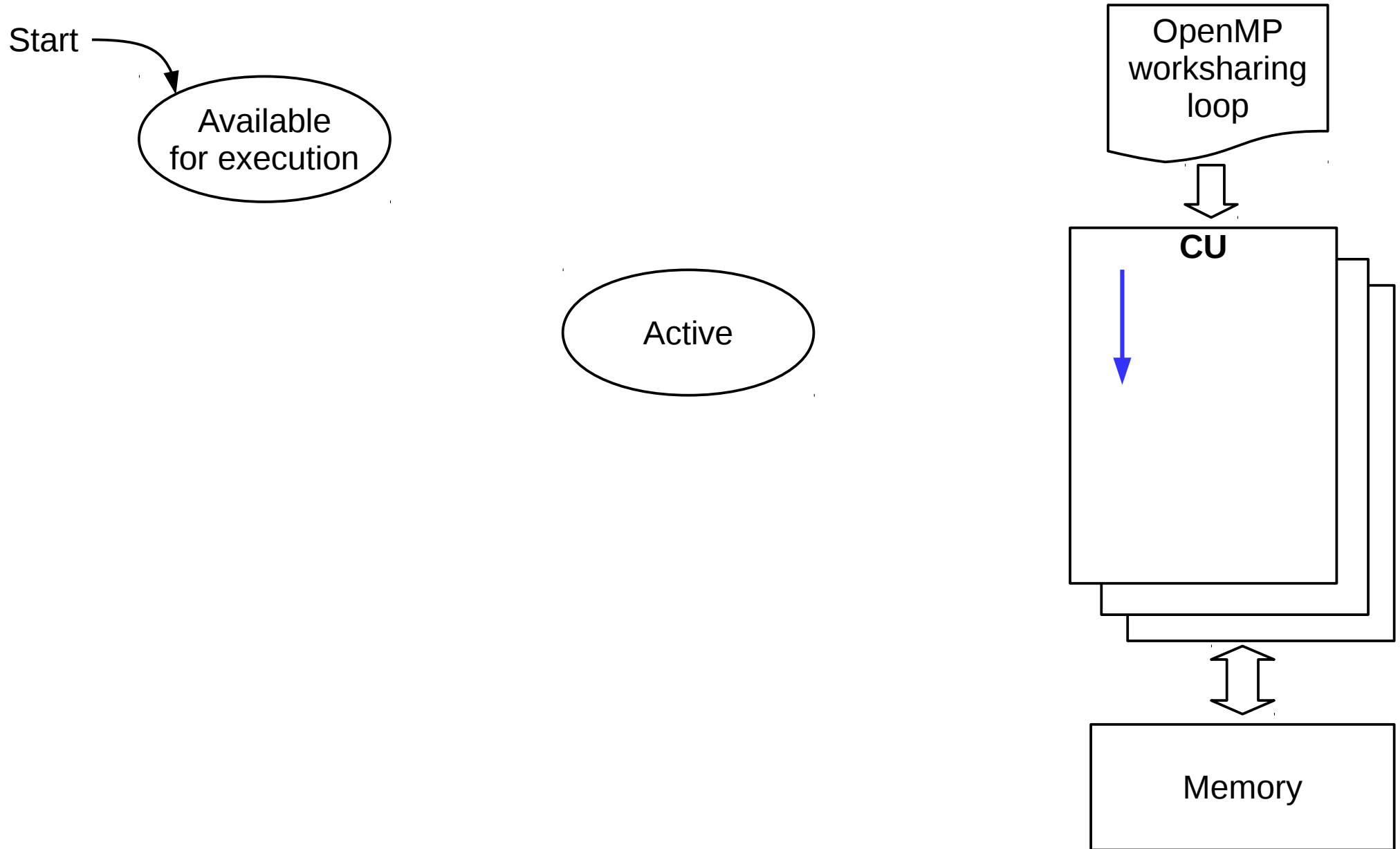
Nymble-OMP

OpenMP
worksharing
loop

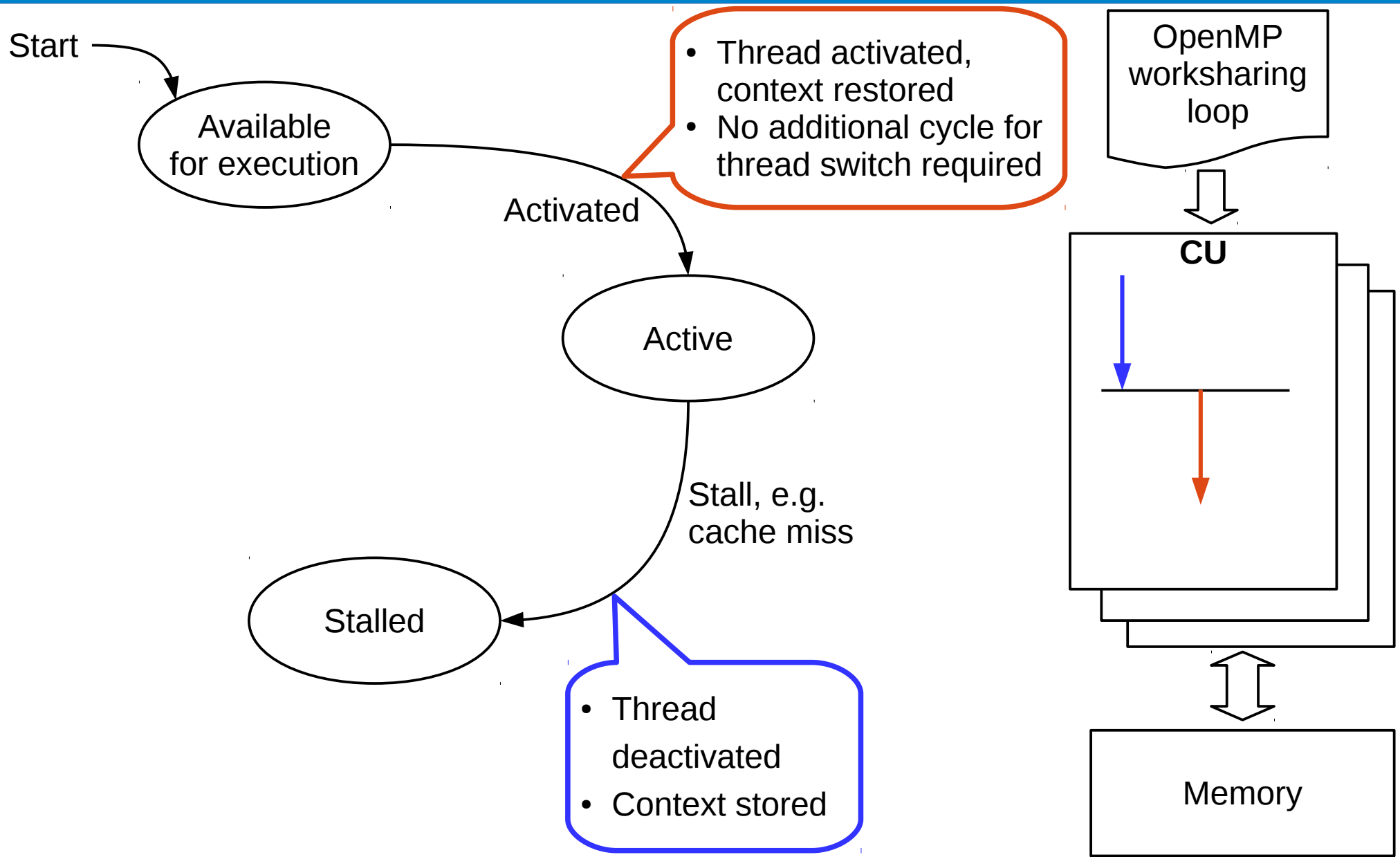
Nymble-Omp



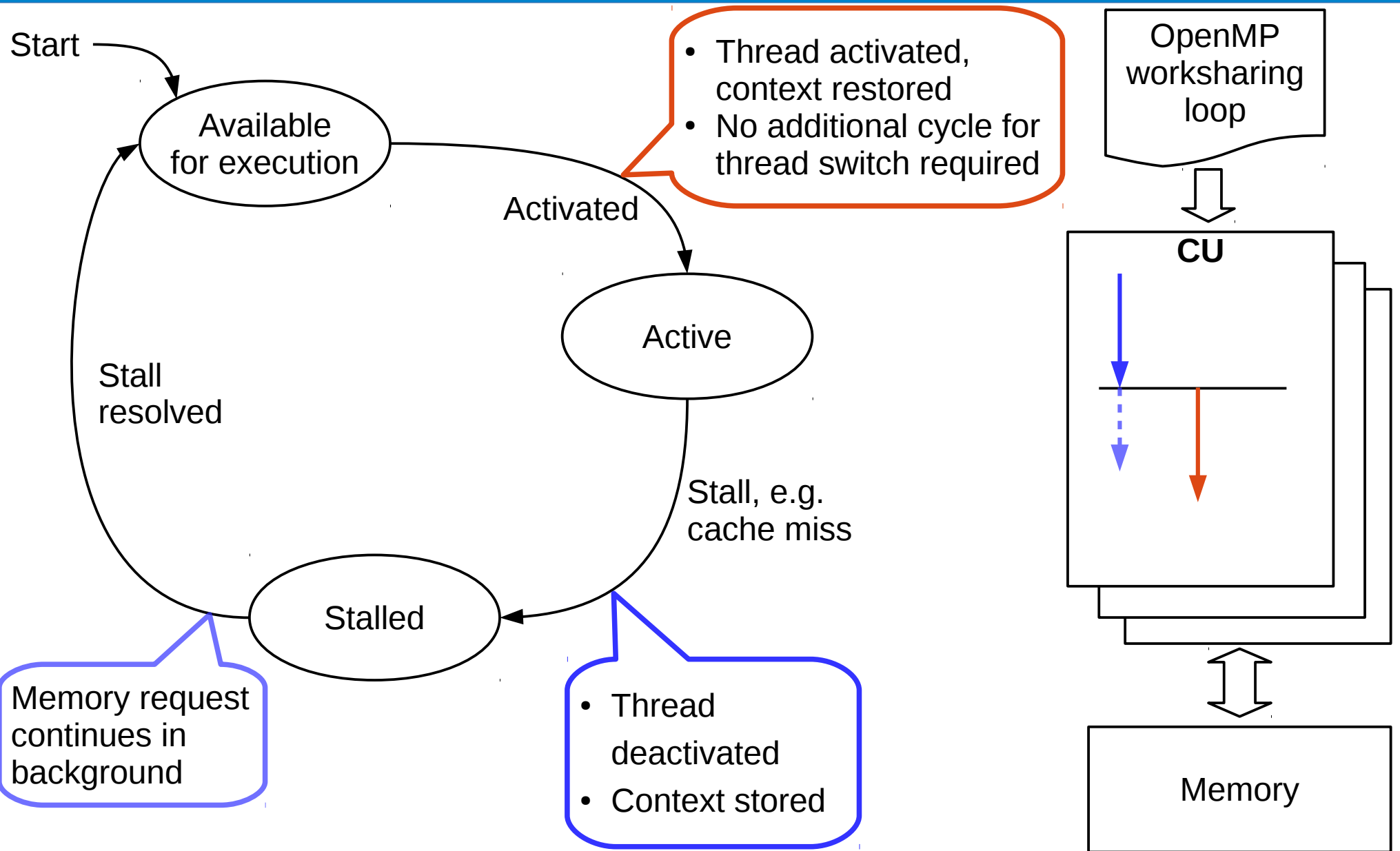
Nymble-Omp



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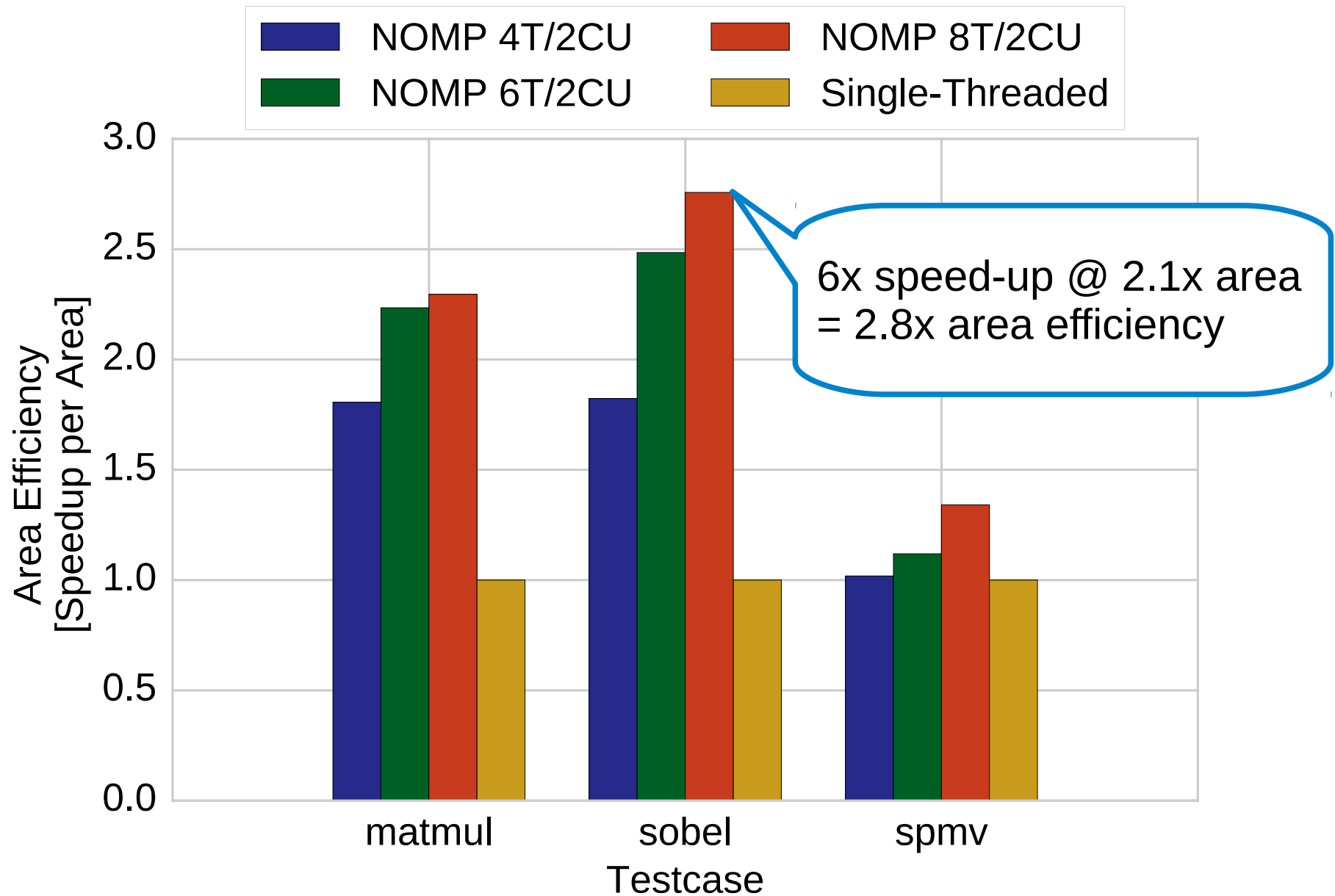
Nymbble-OMP



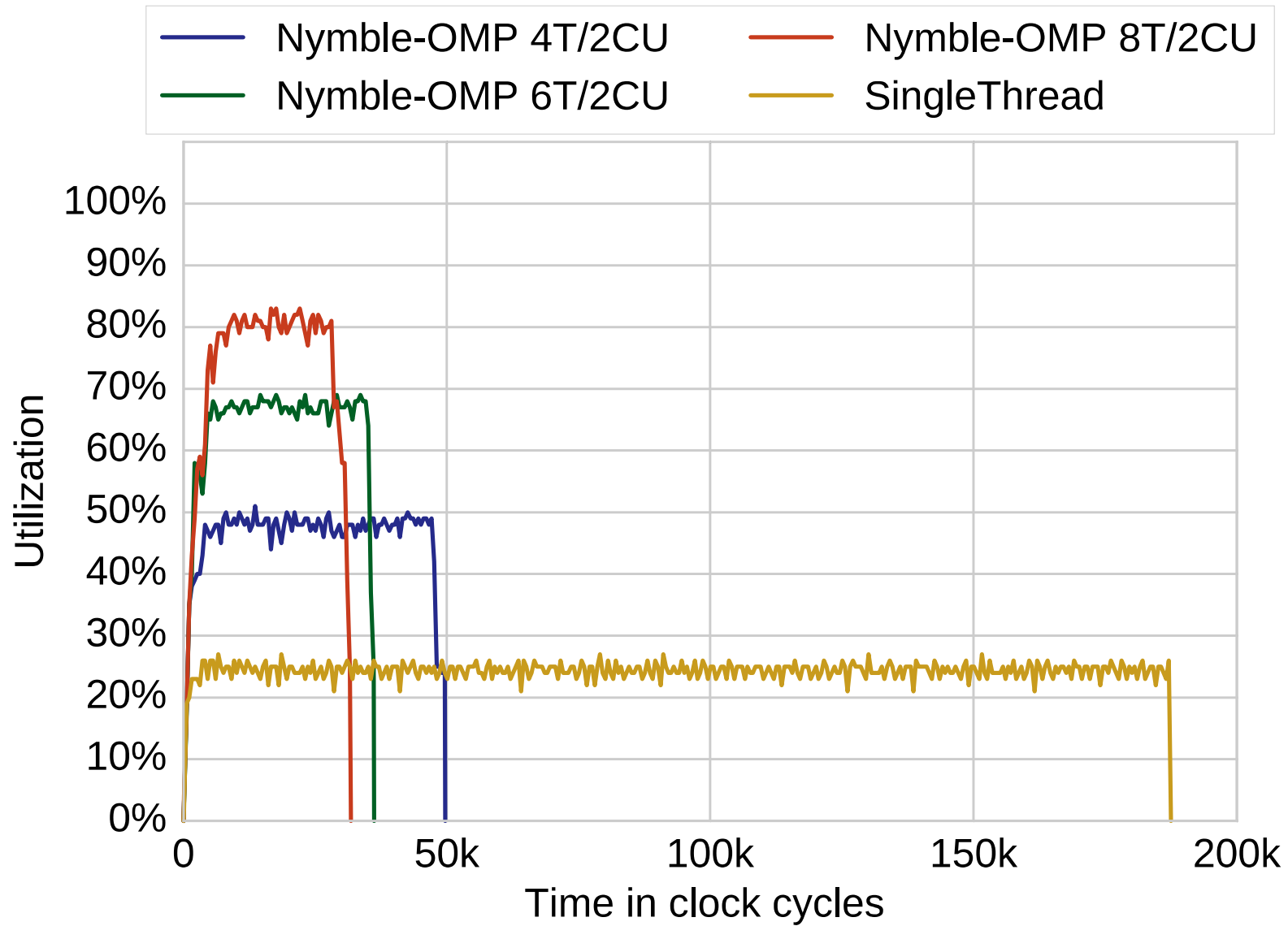
Evaluation

- Evaluation with OpenMP-parallelized matrix algorithms
- Synthesis with 2 CUs, 8 threads (total) for Virtex 7 (XC7VX690T):
 - Clock frequency: 100 MHz
 - Overall FPGA occupancy: 20-25%
 - ~5% overhead of multi-threading compared to single-threaded CU for:
 - Thread Switching Logic
 - Thread Context Storage

Evaluation



Evaluation



Example: sobel

Thank you!

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