Call for Papers
Second International Workshop on
Heterogeneous High-performance Reconfigurable Computing (H²RC)

Held in conjunction with *Supercomputing 2016*
Monday, November 14, 2016
Salt Lake City, UT
http://h2rc.cse.sc.edu

As conventional von-Neumann architectures are suffering from rising power densities, we are facing an era with power, energy efficiency, and cooling as first-class constraints for scalable HPC. FPGAs can tailor the hardware to the application, avoiding overheads and achieving higher hardware efficiency than general-purpose architectures. Leading FPGA manufacturers have recently made a concerted effort to provide a range of higher-level, easier to use high-level programming models for FPGAs.

Such initiatives are already stimulating new interest within the HPC community around the potential advantages of FPGAs over other architectures. With this in mind, this workshop, now its second year, brings together HPC and heterogeneous-computing researchers to demonstrate and share experiences on how newly-available high-level programming models, including OpenCL, are already empowering HPC software developers to directly leverage FPGAs, and to identify future opportunities and needs for research in this area.

Submissions

Submissions are solicited that explore the state of the art in the use of FPGAs in heterogeneous high-performance compute architectures and, at a system level, in data centers and supercomputers. FPGAs may be considered from either or both the distributed, parallel and composable fabric of compute elements or from their dynamic reconfigurability. We particularly encourage submissions which focus on the mapping of algorithms and applications to heterogeneous FPGA-based systems as well as the overall impact of such architectures on the compute capacity, cost, power efficiency, and overall computational capabilities of data centers and supercomputers. Submissions may report on theoretical or applied research, implementation case studies, benchmarks, standards, or any other area that promises to make a significant contribution to our understanding of heterogeneous high-performance reconfigurable computing and will help to shape future research and implementations in this domain. A non-comprehensive list of potential topics of interest is given below:

1. *FPGAs in the Cloud and Data Center:* FPGAs in relation to challenges to Cloud/Data Center/Supercomputing posed by the end of Dennard scaling
2. *Cloud and Data Center Applications:* Exploiting FPGA compute fabric to implement critical cloud/HPC applications
3. *Leveraging Reconfigurability:* Using reconfigurability for new approaches to algorithms used in cloud/HPC applications
4. *Benchmarks:* Compute performance and/or power and cost efficiency for cloud/HPC with heterogeneous architectures using FPGAs
5. *Implementation Studies:* Heterogenous Hardware and Management Infrastructure
6. *Programming Languages/Tools/Frameworks for Heterogeneous High Performance Reconfigurable Computing*
7. *Future-gazing:* New Applications/The Cloud Enabled by Heterogeneous High Performance Reconfigurable Computing, Evolution of Computer Architecture in relation to Heterogeneous High Performance Reconfigurable Computing
8. *Community building*: Standards, consortium activity, open source, education, initiatives to enable and grow Heterogeneous High Performance Reconfigurable Computing

Prospective authors are invited to submit original and unpublished contributions as a one page extended abstract in ACM SIG Proceedings format.

You can submit your contribution(s) through a link on the H2RC website:

http://h2rc.cse.sc.edu

The authors of accepted papers will be invited to present their work at the workshop as a 5 minute talk or as a poster during the poster session.

Important dates:

Submission Deadline:	September 23, 2016 (extended)
Acceptance Notification:	October 14, 2016
Camera-ready Manuscripts Due:	November 4, 2016
Workshop Date:	November 14, 2016

Workshop Format

H2RC is a half-day Monday workshop. It will be comprised of:

- Keynote and invited talks
- Talks selected among paper submissions
- Panel discussion on research opportunities and needs

Organizing Committee

Workshop Organizers:

Michaela Blott, Xilinx
Michael Lysaght, ICHEC
Torsten Hoefler, ETH Zurich
Jason D. Bakos, University of South Carolina

Program Committee:

Franck Cappello, Argonne National Lab
Paul Chow, University of Toronto
Carl Ebeling, Altera
Hans Eberle, NVIDIA
Georgi Gaydadjiev, Maxeler
Alan George, University of Florida
Christoph Hagleitner, IBM
H. Peter Hofstee, IBM Research, Austin
Miriam Leeser, Northeastern University
Wayne Luk, Imperial College
Viktor Prasanna, Univ. of Southern California
Marco Santambrogio, Politecnico Di Milano
Jeffrey Vetter, Oak Ridge National Lab