Call for Papers
First International Workshop on
Heterogeneous High-performance Reconfigurable Computing (H²RC)

Held in conjunction with *Supercomputing 2015*
Sunday, November 15, 2015
Austin, TX
http://h2rc.cse.sc.edu

With Exascale systems on the horizon at the same time that conventional von-Neumann architectures are suffering from rising power densities, we are facing an era with power, energy-efficiency, and cooling as first-class constraints for scalable HPC. FPGAs can tailor the hardware to the application, avoiding overheads of general-purpose architectures. Leading FPGA manufacturers have recently made a concerted effort to provide a range of higher-level, easier to use, high level programming models for FPGAs, including the OpenCL framework, which is already widely used by the HPC community for heterogeneous computing. OpenCL is particularly appealing because it offers the potential for portability to GPUs and Xeon Phi.

Such initiatives are already stimulating new interest within the HPC community around the potential advantages of FPGAs over other architectures in terms of both performance and energy consumption. With this in mind, this will be the first workshop at SC to bring together HPC and heterogeneous-computing researchers to demonstrate and share experiences on how newly-available high-level programming models, including OpenCL, are already empowering HPC software developers to directly leverage FPGAs, and to identify future opportunities and needs for research in this area.

Submissions

Submissions are solicited which explore the state of the art in the use of FPGAs in heterogeneous high-performance compute architectures and, at a system level, in data centers and supercomputers. FPGAs may be considered from either or both the distributed, parallel and composable fabric of compute elements or from their dynamic reconfigurability. We especially encourage submissions which not only consider the implementation of algorithms and applications in FPGAs but concretely relate this to the heterogeneous compute model consisting of differently functioned cooperating compute elements and the overall impact of such architectures on the compute capacity, cost and power efficiency, and computational capabilities of data centers and supercomputers. Submissions may report on theoretical or applied research, implementation case studies, benchmarks, standards, or any other area that promises to make a significant contribution to our understanding of heterogeneous high-performance reconfigurable computing and will help to shape future research and implementations in this domain. A non-comprehensive list of potential topics of interest is given below:

1. *FPGAs in the Cloud and Data Center:* FPGAs in relation to challenges to Cloud/Data Center/Supercomputing posed by the end of Dennard scaling
2. *Cloud and Data Center Applications:* Exploiting FPGA compute fabric to implement critical cloud/HPC applications
3. *Leveraging Reconfigurability:* Using reconfigurability for new approaches to algorithms used in cloud/HPC applications
4. *Benchmarks:* Compute performance and/or power and cost efficiency for cloud/HPC with heterogeneous architectures using FPGAs
5. *Implementation Studies:* Heterogenous Hardware and Management Infrastructure
6. *Programming Languages/Tools/Frameworks for FPGA Heterogeneous Computing*
7. *Future-gazing:* New Applications/The Cloud Enabled by FPGA Heterogeneous Computing, Evolution of Computer Architecture in relation to FPGA Heterogeneous Computing
8. *Community building*: Standards, consortium activity, open source, education, initiatives to enable and grow FPGA Heterogeneous Computing

Prospective authors are invited to submit original and unpublished contributions as 8-page papers. All contributions must be submitted electronically in ACM SIG Proceedings format.

You can submit your contribution(s) by following this EasyChair submission link:

https://easychair.org/conferences/?conf=h2rc

All papers selected for this workshop will be peer-reviewed. The authors of accepted papers will be scheduled to present their work in one of the two lightning talks sessions. Workshop proceedings will be made available online and authors will retain their copyright.

Important dates:

Submission Deadline:	September 14, 2015 (extended)
Acceptance Notification:	October 15, 2015
Camera-ready Manuscripts Due:	November 1, 2015
Workshop Date:	November 15, 2015

Workshop Format

H2RC is a half-day Sunday workshop. It will be comprised of:

- Keynote talks from Jason Cong (UCLA) and Doug Berger (Microsoft Research)
- Panel discussion on research opportunities and needs
- Eight 15-minute talks, selected among paper submissions

Organizing Committee

Workshop Organizers:

Michaela Blott, Xilinx
Michael Leventhal, Xilinx
Michael Lysaght, ICHEC
Torsten Hoefler, ETH Zurich
Kevin Skadron, University of Virginia
Jason D. Bakos, University of South Carolina

Technical Program Co-Chairs:

Deming Chen, UIUC
Kees Vissers, Xilinx Research

Program Committee:

Junwei Bao, Baidu
Michaela Blott, Xilinx
Paul Chow, University of Toronto
Carl Ebeling, Altera
Hans Eberle, NVIDIA
Tarek El-Ghazawi, GWU
Wu Feng, Virginia Tech
Georgi Gaydadjiev, Maxeler
Alan George, University of Florida
Christoph Hagleitner, IBM
Martin Herbordt, Boston University
H. Peter Hofstee, IBM Research, Austin
Miriam Leeser, Northeastern University
Wayne Luk, Imperial College
Walid Najjar, U.C. Riverside
Viktor Prasanna, Univ. of Southern California
Desh Singh, Altera
Mitch Wright, HP