

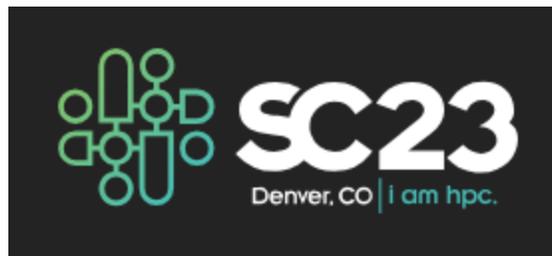
Call for Papers



**Ninth International Workshop on
Heterogeneous High-performance Reconfigurable
Computing (H²RC)**

**November 17, 2023
(Half Day Friday)**

**Held in conjunction with SC23: The
International Conference for High
Performance Computing, Networking,
Storage and Analysis**



<http://h2rc.cse.sc.edu>

Accepted papers will be included in the SC Workshop Proceedings

Submission Deadline

August 7, 2023

(8-page full papers or 2-page extended abstract, see below)

As conventional von-Neumann architectures are suffering from rising power densities, we are facing an era with **power**, **energy efficiency**, and **cooling** as first-class constraints for scalable HPC. FPGAs can tailor the hardware to the application, avoiding overheads and achieving higher hardware efficiency than general-purpose architectures. Leading FPGA manufacturers have recently made a concerted effort to provide a range of higher-level, easier-to-use high-level programming models for FPGAs.

Such initiatives are already stimulating new interest within the HPC community around the potential advantages of FPGAs over other architectures. With this in mind, this workshop, now in its ninth year, brings together HPC and heterogeneous computing researchers to demonstrate and share experiences on how newly-available high-level programming models are already empowering HPC software developers to directly leverage FPGAs and to identify future opportunities and needs for research in this area.

Submission Tracks and Contribution Selection

Submissions are solicited for two tracks:

Track 1: Full-length papers (8 pages, excluding references) for oral presentation and publication in SC Workshop Proceedings.

Track 2: Extended abstracts / talk proposals (2 pages, excluding references) oral presentation without publication.

Track 1 is targeted for technical papers containing a high level of implementation detail and analysis of experimental results. Track 1 is suited for members of the academic and national lab community who prefer to have their work peer-reviewed and included in SC Workshop Proceedings.

Track 2 is targeted for industrial contributions that describe new capabilities and opportunities offered by emerging technologies and products, or work in progress presentations by the academic and national lab community. The emphasis of this track is to initiate a discussion with the audience. These extended abstracts will be made available on the conference website.

All submissions are peer reviewed and evaluated by at least three members of our technical program committee (TPC). From the TPC evaluation of each submission, the organizing committee will select papers for presentation based on a criteria that is **equally weighted** between scientific merit and level of interest and relevance to the HPC community.

Submission Topics

Submissions are solicited that explore the state of the art in the use of FPGAs in heterogeneous high-performance compute architectures and, at a system level, in data centers and supercomputers. FPGAs may be considered from either or both the distributed, parallel and composable fabric of compute elements or from their dynamic reconfigurability. Submissions investigating the use of FPGAs in combination with other devices such as CPU/GPU/APU/DPU are particularly welcomed.

Submissions may report on theoretical or applied research, implementation case studies, benchmarks, standards, or any other area that promises to make a significant contribution to our understanding of heterogeneous high-performance reconfigurable computing and help to shape future research and implementations in this domain. A non-comprehensive list of potential topics of interest is given below:

1. Use of FPGAs to improve performance or efficiency of HPC or data center applications
2. System integration of FPGAs in clouds and distributed HPC systems
3. Leveraging reconfigurability
4. Benchmarks
6. Programming languages, tools, and frameworks
7. Future-gazing

Submission Guidelines

Full papers (Track 1)

Authors should submit original contributions of up to 8 pages (excluding references) in PDF format using the SC23 Linklings portal (<https://submissions.supercomputing.org>), which is also linked from the H2RC website (<https://h2rc.cse.sc.edu>). Submissions must be formatted [using the new proceedings templates and the CCS2012 guide](#). H2RC uses a single blind review process. We support the [SC reproducibility initiative](#) and highly encourage authors to add an artifact description/artifact evaluation appendix of up to 2 additional pages to their paper. All accepted papers will be published in the SC Workshop Proceedings.

Talk proposals (Track 2)

To apply for a talk authors should submit a 2-page extended abstract. The extended abstract will be peer-reviewed and used for deciding on the acceptance of a presentation assignment of a presentation slot, but will be published only on the workshop website but not in the proceedings. The papers shall follow the same formatting instructions as the full papers and have also to be submitted using the Linklings system.

Important dates:

Submission Deadline:	August 7, 2023
Acceptance Notification:	September 8, 2023
Camera-ready Manuscripts Due:	October 13, 2023
Workshop Date:	November 17, 2023

Workshop Format

H²RC is a half-day Friday workshop. It will be comprised of:

- and invited talks
- Talks selected among paper submissions

Workshop Organizers:

Jason D. Bakos, University of South Carolina

Franck Capello, Argonne National Lab

Torsten Hoefler, ETH Zurich

Ken O'Brien, AMD

Christian Plessl, Paderborn University

Technical Program Committee:

TBA